REMARKS

Claims 1-6 are all the claims pending in the application. By this Amendment, Applicants add new claims 5-6.

Claim Rejections – 35 U.S.C. § 101

Claims 1 and 2 are rejected under 35 U.S.C. § 101 as allegedly reciting nonfunctional descriptive material. In view of the amendments to claims 1 and 2, Applicants respectfully submit that the claims comply with the requirements of 35 U.S.C. § 101.

Claim Rejections – 35 U.S.C. § 103

Claims 1-4 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Hasegawa (U.S. Patent No. 6,041,168) (hereinafter Hasegawa '168) in view of Hasegawa (U.S. Patent No. 5,528,511) (hereinafter Hasegawa '511). For at least the following reasons, Applicants respectfully traverse the rejection.

Claims 1-4 recite, among other limitations, that the delay time information is **specific to** an input terminal logical state transition and resulting logical state transition at an output terminal of a logical circuit. The Examiner acknowledges that Hasegawa '168 fails to teach or suggest this feature (Office Action, page 5). The Examiner asserts that Hasegawa '511 teaches this required claim element (Office Action, pages 5-6, citing Hasegawa '511 at Fig. 3; col. 1, lines 28-35; col. 2, lines 30-42; and col. 3, lines 5-26). Applicants respectfully submit that the Examiner is misinterpreting the teachings of Hasegawa '511.

In the cited portions of Hasegawa '511 (e.g., at FIG. 3), a signal waveform for parts of the logic circuit 240 shown in FIG. 2 is shown. Specifically, FIG. 3 shows a timing diagram for two inputs and an output of an OR gate (col. 4, lines 43-45; col. 1, lines 28 -35). However, there

is no delay time information in Hasegawa '511 which is **specific to** an input terminal logical **state transition** (e.g., at input terminals 's' or 'v', see FIGS. 4 and 5) and a resulting logical **state transition** at an output terminal (e.g.,, at output terminal 't'). That is, the nullified states shown in Hasegawa '511, where no further action is required, are explicitly identified with respect to the state transitions at the input terminals and output terminal of the OR gate.

For instance, the delay times shown in FIGS. 12 and 13 are identified between the input terminals 's' or 'v' and the output terminal 't'. On the other hand, with the configuration set forth in claim 1, a target point at which no further delay analysis is required is automatically determined. For example, claim 1 was amended to recite that the delay analyzing module analyzes the delay of the logical circuit based on the delay time information in said delay analysis library (also see new claims 5 and 6).

As such, Applicants respectfully submit that Hasegawa '511 alone, or in combination with Hasegawa '168, does not teach or suggest the above noted features of the claims. Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 103(a) rejection.

New claims

New claims 5-6 are patentable *at least* by virtue of their dependency. Moreover, the prior art of record does not disclose or suggest that the delay analyzing module determines automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit, and when no change in the signal state is determined, the delay analyzing module determines that no further delay analysis needs to be performed as recited in claim 5.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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